



McGill Computational Science and Engineering Seminar



Friday, January 21, 2005 at 2:30 p.m.
McConnell Engineering Bldg. Room 603

Efficient Circuit Simulation using Model Order Reduction

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The recent advances in both digital circuits and analog RF circuits have put new demands on circuit designers. Design automation tools are an integral part of the design process, and an important factor in the current rush to reduce the design cycle and improve the time to market. However, the increasing complexity of modern designs is pushing the limits of current design automation tools. In this presentation, some of the difficulties in the analysis and simulation of RF circuits, and of VLSI interconnect networks will be discussed. Some recent work on projection based model reduction techniques will be presented. Model reduction significantly improves the CPU and memory requirements of circuit simulation, by transforming a large circuit into a much smaller one that captures the essential behaviour of the original circuit, but that is more easily simulated. Numerical examples will be presented to illustrate this approach.

Coffee and snacks will be served in Room 603 after the seminar.